Testbench

module tb\_spi\_state;

// Inputs

reg clk;

reg reset;

reg [15:0]datain;

// Outputs

wire spi\_cs\_l;

wire spi\_sclk;

wire spi\_data;

wire [4:0]counter;

spi\_state dut (

.clk(clk),

.reset(reset),

.counter(counter),

.datain(datain),

.spi\_cs\_l(spi\_cs\_l),

.spi\_sclk(spi\_sclk),

.spi\_data(spi\_data)

);

initial begin

clk = 0;

reset = 1;

datain = 0;

end

always #5 clk=~clk;

initial begin

#10 reset=1'b0;

#10 datain=16'hA569;

#335 datain=16'h2563;

#335 datain=16'h9B63;

#335 datain=16'h6A61;

#335 datain=16'hA265;

#335 datain=16'h7564;

end

endmodule